UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,816	06/30/2003	Bong Soo Kim	40296-0010	8008

26633 7590 11/16/2004

HELLER EHRMAN WHITE & MCAULIFFE LLP
1666 K STREET,NW
SUITE 300
WASHINGTON, DC 20006

EXAMINER	
NGUYEN, THANH T	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,816	KIM ET AL.	
	Examiner	Art Unit	
	Thanh T. Nguyen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,8 and 9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8 and 9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/5/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-5, 8-9 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "the temperature below 600°C" in line 10. There is insufficient antecedent basis for this limitation in the claim. It is suggested to change to --700°C--.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Gardner et al. (U.S. Patent No. 6,144,071).

Referring to figures 5-26, Gardner et al. teaches a method for preventing an out-diffusion of impurities implanted in source/drain regions when forming a transistor of a semiconductor device, comprising the steps of:

Forming a gate electrode (23, gate conductor) on a semiconductor substrate (20);

Ion-implanting impurities (see col. 8, lines 50-63) into the semiconductor substrate (20) the gate electrode as a mask (see figure 1) to form a source/drain junction regions (21, see figure 5);

Forming an oxide film (24) over the gate electrode and the source/drain regions (21) via one of a CVD process (called LPCVD or PECVD, see col. 9, lines 9-20) and a PVD process at a temperature below 700°C (see col. 9, lines 9-20) so as to prevent an out-diffusion of impurities implanted in the source/drain regions (21) toward the surface of the substrate (20), and if the oxide film is formed at the temperature below 600°C performed thermal treatment of the semiconductor substrate at the temperature ranging 600-700°C under a nitrogen gas atmosphere; and (noted that in the condition of the oxide film is deposited at the temperature above 600°C (which is at 650°C-900°C, see col. 9, lines 14-17) therefore the condition below 600°C does not apply.)

Forming a nitride film spacer (26, see figure 7) on a sidewall of the gate electrode (23).

Regarding to claim 2, the step of ion-implanting impurities comprises ion-implanting $_{31}P$ (see col. 8, lines 58-63).

Regarding to claim 3, the step of ion-implanting impurities comprises ion-implanting $_{75}As$ (see col. 8, lines 58-63).

Regarding to claim 8, the thermal treatment is a rapid thermal treatment performed for 1-5 minutes or thermal treatment performed in a furnace for a time period ranging form 1 minutes -6 hours (see col. 9, lines 34-45).

Regarding to claim 9, the thermal treatment is in a furnace for 1 minutes to 6 hours (see col. 9, lines 34-45).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2-5, 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. (U.S. Patent No. 6,144,071) as applied to claims 1 above in view of Kadosh et al. (U.S. Patent No. 6,589,849).

Referring to figures 5-26, Gardner et al. teaches a method for preventing an out-diffusion of impurities implanted in source/drain regions when forming a transistor of a semiconductor device, comprising the steps of:

Forming a gate electrode (23, gate conductor) on a semiconductor substrate (20);

Ion-implanting impurities (see col. 8, lines 50-63) into the semiconductor substrate (20) the gate electrode as a mask (see figure 1) to form a source/drain junction regions (21, see figure 5);

Forming an oxide film (24) over the gate electrode and the source/drain regions (21) via one of a CVD process and a PVD process at a temperature below 700 °C (see col. 9, lines 9-20) so as to prevent an out-diffusion of impurities implanted in the source/drain regions (21) toward the surface of the substrate (20), and if the oxide film is formed at the temperature below 600°C performed thermal treatment of the semiconductor substrate at the temperature ranging 600-700°C under a nitrogen gas atmosphere; and (noted that in the process the condition of the oxide film is deposited at the temperature above 600°C (which is at 650°C-900°C, see col. 9, lines 14-17) therefore the condition below 600°C does not apply.)

Forming a nitride film spacer (26, see figure 7) on a sidewall of the gate electrode (23).

Regarding to claim 2, the step of ion-implanting impurities comprises ion-implanting $_{31}P$ (see col. 8, lines 58-63).

Regarding to claim 3, the step of ion-implanting impurities comprises ion-implanting $_{75}As$ (see col. 8, lines 58-63).

Regarding to claim 5, the ion-implanting process is performed using a single-type equipment without wafer tilt and rotation (see figure 1).

Regarding to claim 8, the thermal treatment is a rapid thermal treatment performed for 1-5 minutes or thermal treatment performed in a furnace for a time period ranging form 1 minutes -6 hours (see col. 9, lines 34-45).

Regarding to claim 9, the thermal treatment is in a furnace for 1 minutes to 6 hours (see col. 9, lines 34-45).

However, Gardner et al. does not teach implantation energy range and the doses range, implanting process using a single-type equipment with wafer tilt of 1o and in a bi-rotation or a quardruple-rotation configuration, and the temperature range.

Referring to figures 2-6, Kadosh et al. teaches a method of implanting the gate electrode (18) by using N-type dopant materials such as arsenic or phosphorus with the doses range of $1x10^{12}$-$1x5^{13}$ ions/cm^2 at an angle approximately 0-60°C (called tilt) at the energy range approximately 10-40keV (see col. 6, lines 38-48).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would implanting the gate electrode by using N-type dopant materials such as arsenic or phosphorus with the doses range of $1x10^{12}$-$1x5^{13}$ ions/cm^2 at an angle approximately 0-60°C at the energy range approximately 10-40keV in process of Gardner et al. as taught by Kadosh et al. because would reduce threshold voltage roll-off characteristic and improve control of short-channel effect, lower the leakage currents.

The temperature range are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in In re Aller, the selection of reaction parameters such as temperature and concentration would have been obvious:

> "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."

In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

Therefore, one of ordinary skill in the requisite art at the time the invention was made would have used any temperature range suitable to the method in process of Gardner et al. in order to optimize the process.

The specification contains no disclosure of either the critical nature of the claimed temperature (i.e.-thermal treatment of the semiconductor substrate at a temperature ranging from 600-700°C) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the applicant must show that the chosen limitations are critical. In re Woodruff, 919 F.2d 1575, 1578 (FED. Cir. 1990).

Response to Arguments

Applicant's arguments with respect to claims 1-5, 8-9 have been considered but are moot in view of the new ground(s) of rejection.

Applicant contends that Gardner fails to disclose or suggest performing thermal treatment of the substrate at a temperature ranging from 600-700oC under a nitrogen gas atmosphere if the oxide film is formed at temperature below 600°C. In response to applicant that since the condition of the oxide formed at the temperature of above 600°C (which is at 650°C-900°C, see col. 9, lines 14-17) therefore the condition below 600°C does not need to apply).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this

Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached on (571) 272-1702. The fax phone number for this Group is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (**See MPEP 203.08**).

Thanh Nguyen
Patent Examiner
Patent Examining Group 2800